CLAIMS

1. A testable electronic system including testable elements having standardized test interfaces for organizing the elements in chains which behave like shift registers to ensure the exchange of test information, each element being either a component (10) including an identifier characterizing the behavior of the test of the component and accessible by the test interface of the component, or a switch (24) for organizing a chain in sub-chains which can be individually selected through channels of the switch, the system including master switches (24) which define respective sub-sets (20) of elements, a specific channel of each master switch being reserved to access an identifier (22) characterizing the test organization of the associated sub-set.

2. The system of claim 1, wherein the channels of each master switch (24), other than the reserved one, are connected to sub-chains that can include, in an arbitrary organization, one or more elements or master switches.

3. The system of claim 1, wherein each sub-set corresponds to a printed circuit board (20) including a connector (26) which connects its master switch (24) to a channel of a master switch of another board, all the boards being connected, through interposed master switches, to a channel of a master switch of a single interface board (28) through which the system is tested.

4. The system of claim 3, including a data base associating:

with each distinct component identifier (10), a set of test vectors and of corresponding expected results; and

with each distinct sub-set or board identifier (22), information indicating the organization of the board's sub-chains, a set of test vectors associated with each sub-chain of the board, and the corresponding expected results.

5. A method of use of the testable electronic system of claim 4, including, to test a predetermined board, the step of scanning the graph formed by the connections between boards (20) until a path to the predetermined board is found, said graph

being scanned by scanning each board that is found connected to a preceding board by using the information associated, in the data base, with the identifier (22) of the preceding board.

6. The method of claim 5, wherein the graph is scanned along an Euler path for linking all the boards (20) together, the algorithm for establishing the Euler path being modified so that the Euler path can pass more than once through a same channel.

7. The method of claim 5, including the step of testing the predetermined board by using vectors associated, in the data base, with the identifier (22) of the predetermined board, said vectors being provided, and the corresponding results being retrieved through the path that was found.

8. The method of claim 5, including the following steps:

- searching for a predetermined component (10) by reading the identifiers of the components in the sub-chains of the predetermined board; and

- testing the predetermined component by using test vectors associated, in the data base, with the component's identifier.